

(Use several sheets if necessary)

**YO999-408 CIP**

**Not Yet Assigned**

Cohen et al.

**Concurrently Herewith**

**Not Yet Assigned**

[illegible][illegible]

Erik Kuchir

2/1/02

**SHEET 1 OF 1**

15 (Use several sheets if necessary)

Application Number	09/902,483
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**Applicant(s)**  
**Cabral, Jr., et al.**

**Filing Date** **July 11, 2001**

Group Art Unit	2813
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[illegible][illegible]

Ek	U.S. Patent Application No. 09/515,033, YOR900-0044US1, "Method For Self-Aligned Formation Of Silicide Contacts Using Metal Silicon Alloys For Limited Silicon Consumption And For Reduction Of Bridging", pp. 1-21, and Figs. 1A-3B. now U.S. Patent 6,323,130
Ek	Lisa T. Su, Melanie J. Sherony, Hang Hu, James E. Chung, and Dimitri A. Antoniadis; "Optimization of Series Resistance in Sub-0.2, um SOI MOSFET's; IEEE Electron Device Letters, Vol. 15, No. 9, September 1994; pages 363-365.

Eric Kohn

2/1/02

**Form PTO-A820**  
**(also form PTO-1449)**

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OF

# INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

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YO999-4 TIP

Application Number  
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Applicant(s)  
Cabral, Jr. et al.

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Group Art Unit  
2813

\*EXAMINER  
INITIAL

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EA

T. Yoshitomi, M. Saito, T. Ohguro, M. Ono, H.S. Momose, and H. Iwai; "Silicided Silicon-Sidewall Source and Drain (S4D) structure for high-performance 75-nm gate length pMOSFETs; 1995 Symposium on VLSI Technology Digest of Technical Papers; 0-7803-2602-4/95; pages 11 and 12.

EA

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EXAMINER

*Erik...*

DATE CONSIDERED

2/1/02

\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.